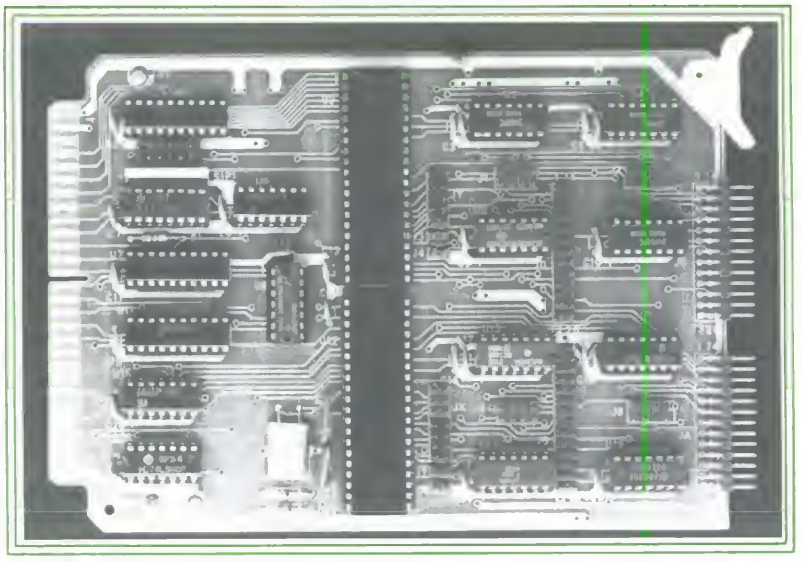


FEATURES

- STD-Z80 Bus Compatible
- Four Full Duplex RS-232-C serial ports
- Multi-protocol — software selectable
- Synchronous, Asynchronous, HDLC, SDLC
- CRC Generation and Checking
- NRZ, NRZI, FM data encoding/decoding
- Programmable baud rates for each port
- Local Loopback and Auto Echo Modes
- Two fully independent channels, each containing:
  - — One data communication equipment (DCE) port
  - — One data terminal equipment (DTE) port
- 4 MHz operation
- 1 Year Warranty

DESCRIPTION

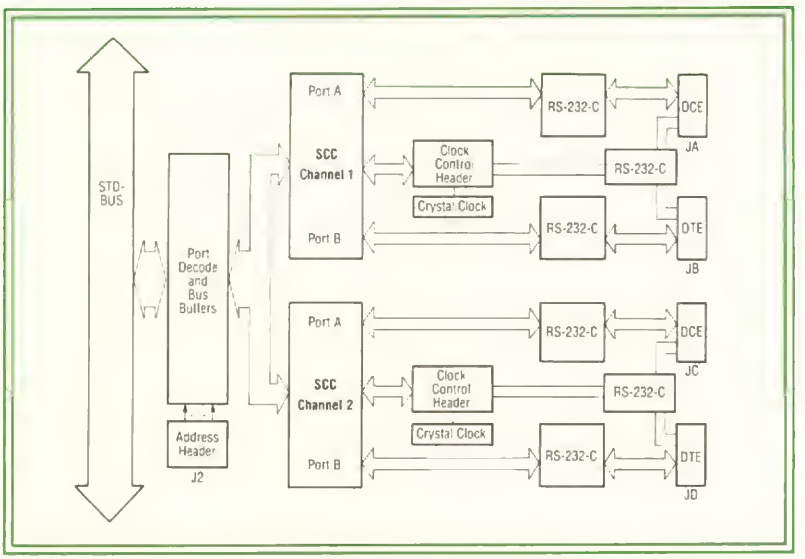
The Colex STD-SIO4 is a general purpose serial I/O board for the STD Bus. The card contains two high performance ZILOG Z8530 SCC devices, each one combining the features of a SIO device in addition to programmable NRZ, NRZI and FM data encoders/decoders, a digital phase locked loop for clock recovery and baud rate generator. These on-chip features allow a dramatic reduction in external logic to support an extremely wide range of serial communications applications. All necessary support and control circuitry to provide four complete and separately configurable serial I/O (RS-232-C) ports is included on the board.

The basic role of the 8530 device is parallel to serial conversion, serial to parallel conversion, and control of the process. Within this role, it is software configurable for a wide range of variations on the primary task of serial communication and can be optomized for specific serial communication applications. The 8530 SCC is an extremely versatile and powerful device and the design of the STD-SIO4 board allows use of its many features either by software or jumper selection.

Each port is configured to the EIA standard RS-232-C specification DTE and DCE serial communications operation. All ports support a full complement of handshake signals for connection to a modem. Jumper selected options allow the configuration of each port for almost any synchronous clocking arrangement desired. In addition, jumpers are provided for bypassing the Data Carrier Detect (DCD) input of each port if the external device does not support this signal.

COLEX AMERICA, INC. P.O. Box 801462, Dallas, Texas 75380, United States 214/458-2779
COLEX U.K., LTD. Index House, Ascot Berks, SL57EU, England, (0990)-23377
COLEX ASIA PACIFIC Luk Hop Industrial Bldg., 15th Floor, 8 Luk Hop St., San Po Kong, Kowloon, Hong Kong 3/7265651

STD-SIO4 BLOCK DIAGRAM



SPECIFICATIONS

ELECTRICAL

- System Bus: STD-Z80
  Inputs: one 74LS load maximum
  Outputs: $I_{OH} = -3mA$ min @ 2.4 volts
  $I_{OL} = 24mA$ min @ 0.5 volts
- System Clock: 4 MHz
- Data Bus: 8-bit, bi-directional
- Address Bus: 16-bit
- I/O Address: Any 8 Sequential Ports
- I/O Capacity: 4 EIA RS-232-C serial ports
- Interrupts: All three Z80 modes
- System Interrupt Units: 2 SIUs
- Operating Temperature: 0° to 60° C.
- Power Requirement @ 25° C:

Parameter	Condition	Min	Typ.	Max.	Units
V_{CC}	—	4.75	5.00	5.25	volts
I_{CC}	5vdc	—	412	573	mA
V_{CC}	—	11.4	12.0	12.6	volts
I_{CC}	12vdc	—	76	100	mA
V_{CC}	—	−11.4	−12.0	−12.6	volts
I_{CC}	−12vdc	—	72	92	mA

MECHANICAL

- Card Dimensions:

Form Factor	H	W	L	Units
STD-Bus	0.60	4.5	6.5	inches

- PC Board Thickness: 0.062 inch
- Connectors:
  STD-Z80 Bus: 56 pin, 0.125 inch centers
  Serial: 26 pin, dual row, 0.100 inch grid

ORDERING INFORMATION

Part Number	Description
STD-SIO4	4 Channel Serial Communications Card
STM-SIO4	STD-SIO4 Technical Manual

COLEX

SIO4

FEATURES

- ☐ STD-Z80 Bus Compatible
- ☐ Four Full Duplex RS-232-C Serial Ports
- ☐ Multi-protocol - Software Selectable
- ☐ Synchronous, Asynchronous, HDLC/SDLC
- ☐ CRC Generation and Checking
- ☐ NRZ, NRZI, FM Data Encoding/Decoding
- ☐ Programmable Baud Rates for Each Port
- ☐ Local Loopback and Auto Echo Modes
- ☐ Two Fully Independent Channels, Each Containing:
  - One Data Communication Equipment (DCE) Port
  - One Data Terminal Equipment (DTE) Port
- ☐ 4 MHz Operation
- ☐ 1 Year Warranty

DESCRIPTION

STD–SIO4

The COLEX STD–SIO4 is a general purpose serial I/O board for the STD Bus. The card contains two high performance ZILOG Z8530 SCC devices, each one combining the features of a SIO device in addition to programmable NRZ, NRZI, and FM data encoders/decoders, dual on chip programmable baud rate generators, and a digital phase locked loop for clock recovery. These on chip features allow a dramatic reduction in external logic to support an extremely wide range of serial communications applications. All necessary support and control circuitry to provide four complete and separately configurable serial I/O (RS–232–C) ports is included on the board.

The basic role of the 8530 device is parallel to serial conversion, serial to parallel conversion, and control of the process. Within this role, it is software configurable for a wide range of variations on the primary task of serial communication and can be optimized for specific serial communication applications. The 8530 SCC is an extremely versatile and powerful device. The design of the STD–SIO4 board allows use of its many features, either by software or jumper selection.

The board's four serial ports are divided into two channels of two ports each. Each channel is provided by one of the SCC devices and consists of port A and port B as well as clock, control, interrupt, and status lines. Port A of each channel is configured as a Data Terminal Equipment (DTE) port and port B of each channel is configured as a Data Communication Equipment (DCE) port. Both SCC devices contain an independently programmable baud rate generator for each port allowing all four ports on the card to be run at different baud rates as well as other options such as different baud rates for receive and transmit through the same port as the user desires.

Each of the four ports are capable of operation under the following protocols: asynchronous, synchronous and synchronous bit or byte oriented protocols such as BISYNC, SDLC, HDLC, etc. NRZ,

NRZI, and FM encoding/decoding are supported as well. Within each operating mode, there are provisions for protocol variations by checking odd/even parity, character insertion and deletion, CRC generation and checking, break and abort generation and detection, and many other protocol dependent features. In addition, each port has full modem control capability.

Each port is configured to the ANSI standard RS-232-C specification for DTE and DCE serial communications operation. All ports support a full complement of handshake signals for connection to a modem. Jumper selected options allow the configuration of each port for almost any synchronous clocking arrangement desired. In addition, jumpers are provided for bypassing the Data Carrier Detect (DCD) input of each port if the external device does not support this signal.

Z80 interrupt mode 2 operation is supported by the SCC devices which have a series of on-chip registers for storage of vectors and status and control registers allowing interrupt arbitration. The STD-SI04 board is configured for participation in daisy-chained interrupt control and arbitration among other boards on the STD-Z80 Bus.

Programmable configuration of the STD-SI04 by the system CPU is normally done at card initialization at which time all control and data registers are loaded. Control register contents may be examined and/or changed by the system CPU at any time.

Items to be loaded include baud rates, communication protocol, interrupt vectors, prioritization instructions, and so on. Other options are selected by strapping pins on control headers. Care has been taken to ensure that jumper connections occur directly across the header wherever practical allowing options to be selected by simple insertion of Berg™ type straps. In these and other cases, wire-wrapping is satisfactory as well.

For detailed operation and programming procedures, baud rate selection, and other information on the 8530 SCC device, serial communications protocols, specific data on support devices, programming and operation of interrupt controllers, or detailed description or analysis beyond what is presented here, consult the various 7400 TTL data books, serial communications handbook, and Zilog Z80® CPU and SCC technical manuals and data sheets.

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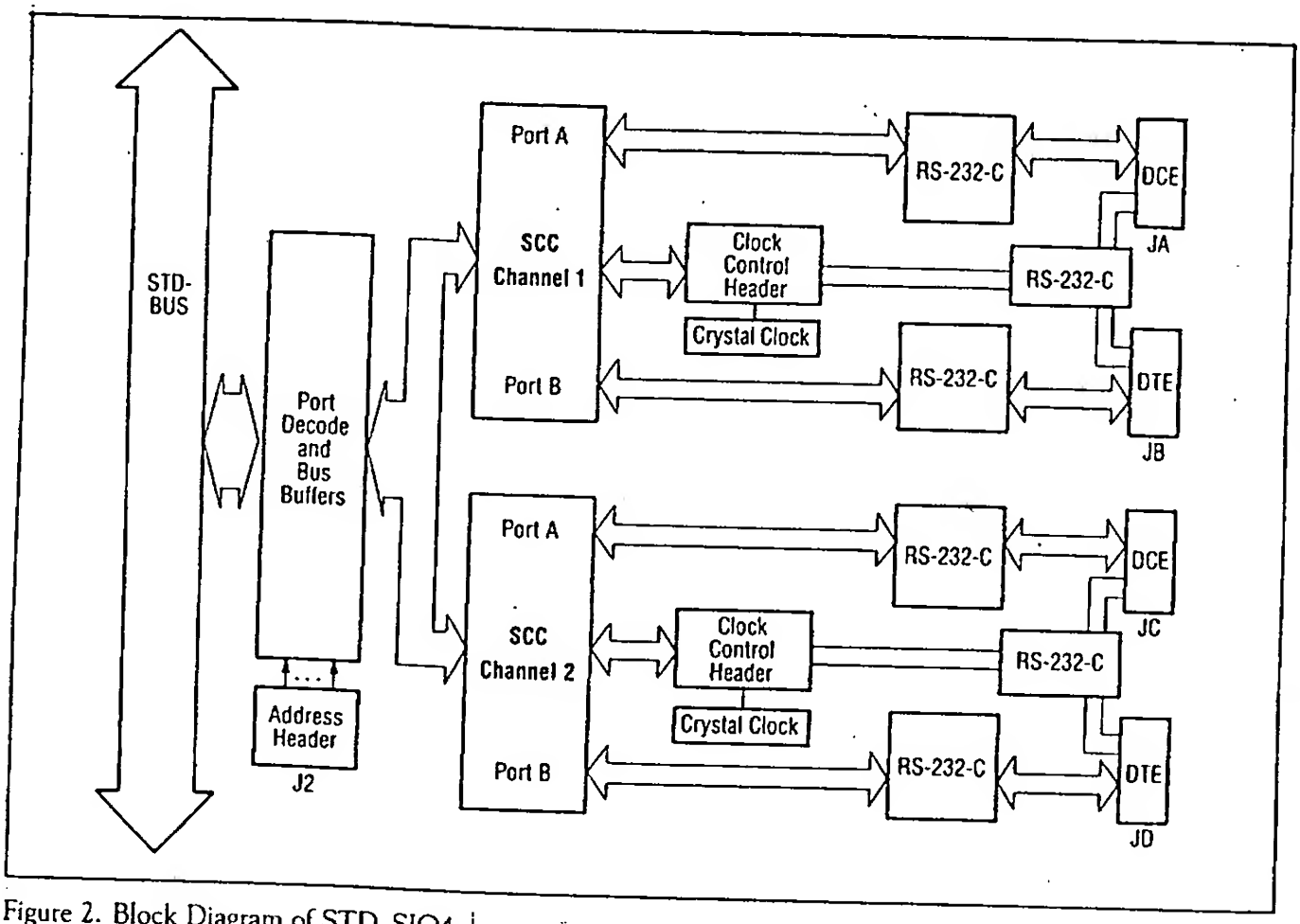


Figure 2. Block Diagram of STD–SIO4

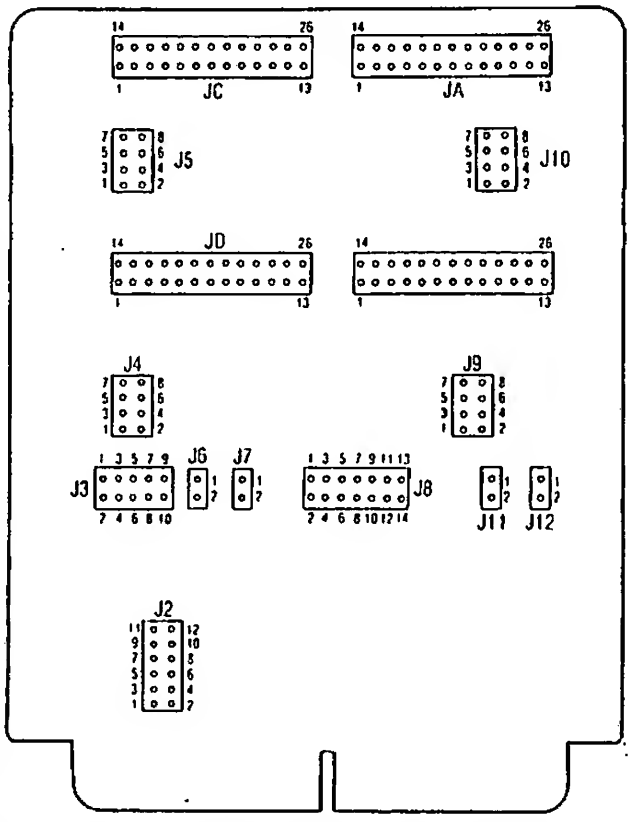


Figure 3. STD–SIO4 Connector and Header Locations

OPTION SELECTION

Jumper selectable options, port addresses, and so on are selected by inserting a shorting strap across a pair of control header pins. In most cases, the pins are situated directly across the header from each other allowing the option to be selected by inserting a Berg type strap. In these and other cases, wire-wrapping is satisfactory as well.

The STD-SIO4 is addressed by any 8 sequential ports. The port address selection for the entire card is selected by jumpers installed on address header J-2. A jumper installed on the header represents a logic 0 as detailed in figure 4. Specific addresses decoded by the SCC devices for each port are shown in figure 5.

Beyond port addressing, each of the two channels is completely independent, is configured by separate control headers, and therefore must be configured through jumpers separately. The reference designators of the control headers are J-8 for channel ONE, and J-3 for channel TWO.

Each port has options that allow a wide variety of synchronous input/output clock configurations to be selected. These configurations are implemented by installing the appropriate jumpers in the sync clock header J-5 (port A) and J-4 (port B) for channel ONE, and J-10 (Port A) and J-9 (Port B) for channel TWO.

PORT ASSIGNMENTS

Address Line	J-2 Pin Pair	Select 0	Select 1
A7	9-10	Jumpered	Open
A6	7-8	Jumpered	Open
A5	5-6	Jumpered	Open
A4	3-4	Jumpered	Open
A3	1-2	Jumpered	Open
IOEXP	11-12	Jumpered	Open

Figure 4. STD-SIO4 Address Selection Header

Port Address				Device
A7-A3	A2	A1	A0	
X	0	0	0	SCC1 (Channel One) Port B Control/Status
X	0	0	1	SCC1 (Channel One) Port A Control/Status
X	0	1	0	SCC1 (Channel One) Port B Data (Terminal)
X	0	1	1	SCC1 (Channel One) Port A Data (Printer)
X	1	0	0	SCC2 (Channel Two) Port B Control/Status
X	1	0	1	SCC2 (Channel Two) Port A Control/Status
X	1	1	0	SCC2 (Channel Two) Port B Data (Terminal)
X	1	1	1	SCC2 (Channel Two) Port A Data (Printer)

Figure 5. STD–SIO4 Port Assignments

STD-SIO4 CLOCK SELECTION

The Z8530 SCC device contains two internal baud rate generators. Only an external clock signal source is required. This source can have a wide variety of origins including a crystal, an oscillator module, System Bus Clock, synchronous communications devices, or some other external source. The baud rate generators divide this signal by a programmable time constant to arrive at the desired rate. The output of the baud rate generator can be used as either the receive clock, transmit clock, or both.

The STD–SIO4 is supplied with a 3.6864 MHz crystal installed on the board allowing all popular baud rates to be generated. Jumpers allow an extremely wide variety of clock combinations to be selected for each port on the board. Figure 6 details logic and strapping locations for Channel ONE (figure 7 for Channel TWO) clock options selection.

Two additional sync clock headers for each channel allow the widest flexibility for configuring the board for synchronous communications. These sync clock headers determine the source of both transmit and receive clocks for each of the four ports. Consult the Zilog data books and COLEX application notes to identify jumpering for specific applications.

SIGNAL CONVENTION

The EIA RS-232-C standard defines machine interfaces as either DTE or DCE. Business machines are defined as Data Terminal Equipment (DTE), and communications equipment is defined as Data Communications Equipment (DCE). The STD–SIO4 is designed to support DTE with port A (both channels) and DCE with port B (both channels). Transmit data, receive data, and all appropriate control signals are provided by the board in accordance with the EIA specifications for signal direction and electrical levels.

The DCD headers permit a jumper to be installed to enable the Data Carrier Detect (DCD) logic in the SCC device. This jumper is required if the DTE does not supply a DTR input and if the DCE does not supply a DSR input. Figure 8 details the correspondence between the individual ports, their output connectors, DCD, and sync clock headers.

Serial Port	Output Connector	DCD Header	Sync Clock Header
Channel 1, PORT A	J-A	J-12	J-5
Channel 1, PORT B	J-B	J-11	J-4
Channel 2, PORT A	J-C	J-7	J-10
Channel 2, PORT B	J-D	J-6	J-9

Figure 8. Port Connector and Header Table

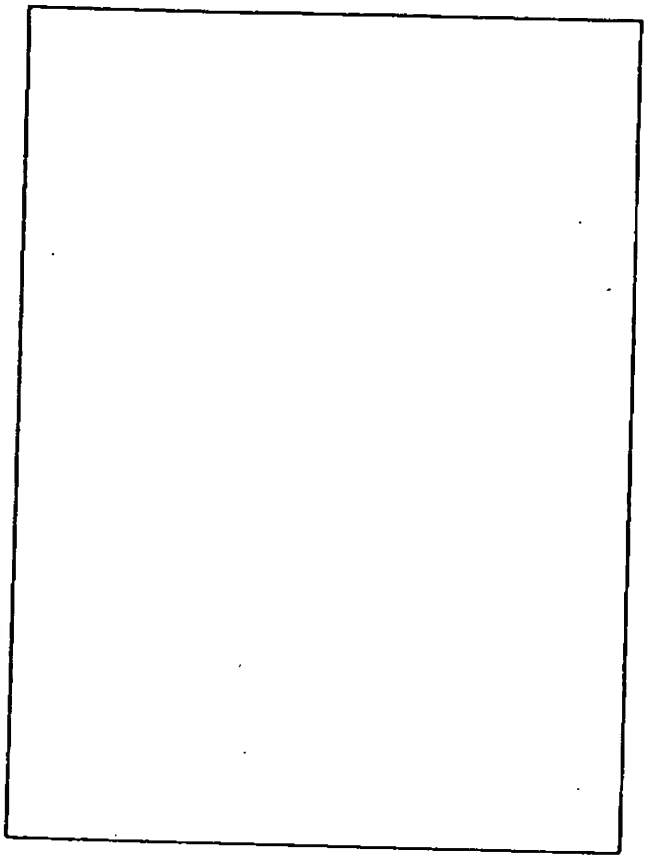


Figure 6. STD-SI04 Channel 1 Jumper Options

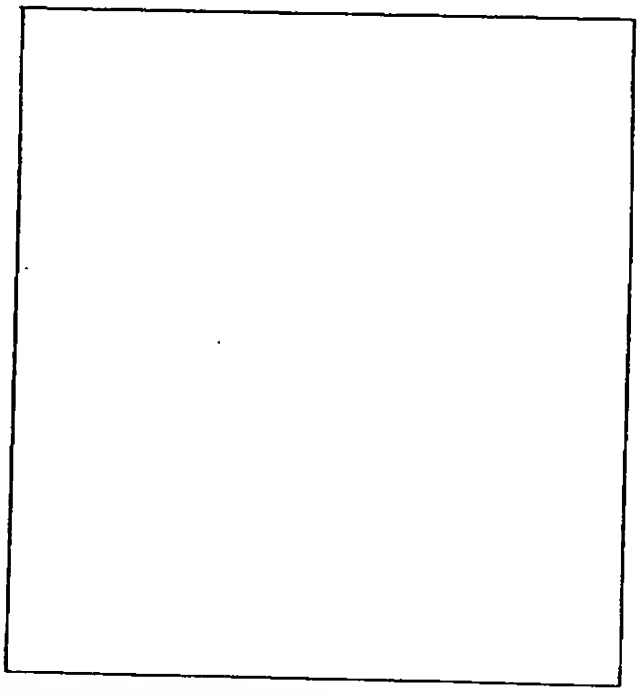


Figure 7. STD-SI04 Channel 2 Jumper Options

PORT OUTPUT CONNECTORS

Each of the four serial ports is configured to be an RS-232-C type interface and is brought out to a 26-pin, dual row, 0.100 inch grid connector. Figure 9 shows output connector pin-out and signal names.

Signal Name	Pin #	Header	Pin #	Signal Name
GND	1	o o	14	–
RX (BA)	2	o o	15	TSE (DB)
TX (BB)	3	o o	16	–
RTS (CA)	4	o o	17	RSE (DD)
CTS (CB)	5	o o	18	–
DSR (CC)	6	o o	19	–
AUX GND	7	o o	20	DTR (CD)
RSLD (CF)	8	o o	21	–
–	9	o o	22	–
–	10	o o	23	–
–	11	o o	24	TSE (DA)
–	12	o o	25	–
–	13	o o	26	–

Serial Communication Handshake Signals
TXD (BA) Transmit Data
RXD (BB) Receive Data
RTS (CA) Request to Send
CTS (CB) Clear to Send
DSR (CC) Data Set Ready
DTR (CD) Data Terminal Ready
TSE (DA) Transmit Signal Element Timing (DTE source)
RSE (DD) Receiver Signal Element Timing (DCE source)
TSE (DB) Transmission Signal Element Timing (DCE source)

Figure 9. Output Connector Pinout and Signal Names

STD-Z80 Bus Connector

Bus Connector: 56-pin dual edge connector, 0.125 contact centers

Signal Name	Pin Numbers		Signal Name
+5 VDC	2	1	+5 VDC
GROUND	4	3	GROUND
N/C	6	5	N/C
D7	8	7	D3
D6	10	9	D2
D5	12	11	D1
D4	14	13	D0
N/C	16	15	A7
N/C	18	17	A6
N/C	20	19	A5
N/C	22	21	A4
N/C	24	23	A3
N/C	26	25	A2
N/C	28	27	A1
N/C	30	29	A0
RD*	32	31	WR*
MEMRQ*	34	33	IORQ*
N/C	36	35	IOEXP
N/C	38	37	N/C
N/C	40	39	STATUSI*
N/C	42	41	N/C
INTRQ*	44	43	INTAK*
N/C	46	45	N/C
N/C	48	47	SYSRESET*
N/C	50	49	CLOCK*
PCI	52	51	PCO
N/C	54	53	N/C
N/C	56	55	N/C

Figure 10. STD-Z80 Parallel I/O Connector

SPECIFICATIONS

ELECTRICAL

- ☐ System Bus: STD-Z80
- ☐ System Clock: 4 MHz
- ☐ Data Bus: 8-bit, bi-directional
- ☐ Address Bus: 16-bit
- ☐ Signal Loading: Inputs: One 74LS maximum
  Outputs: I_{OH}=-3mA min @ 2.4 volts
  I_{OL}=24mA min @ 0.5 volts
- ☐ I/O Address: Any 8 sequential ports
- ☐ I/O Capacity: 4 EIA RS-232-C serial ports
- ☐ Interrupts: All three Z80 modes
- ☐ System Interrupt Units: 2 SIUs
- ☐ Operating Temperature: 0°C to 60°C
- ☐ Power Requirement: @ 25°C

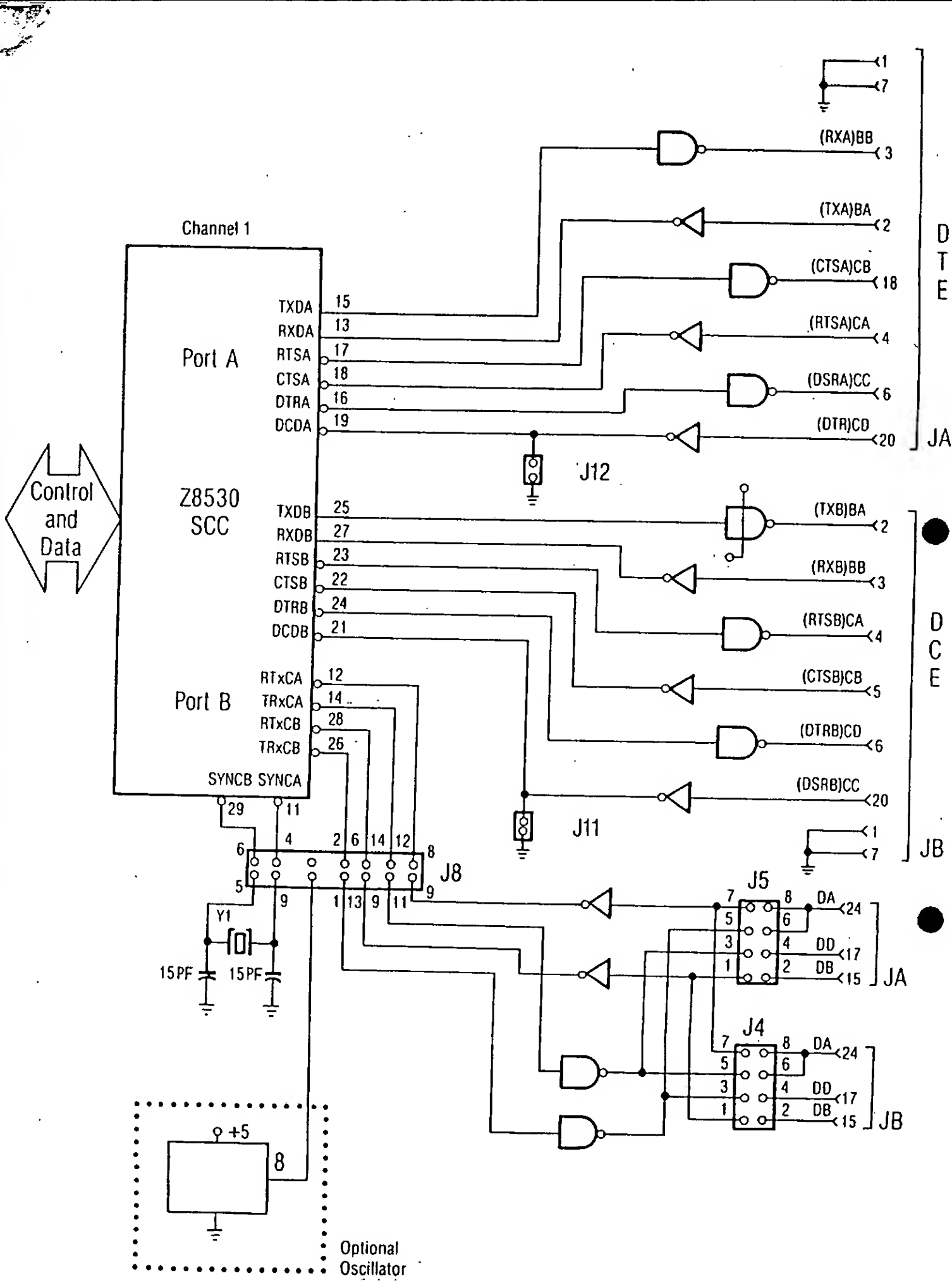
Parameter	Condition	Min.	Typ.	Max.	Units
V_{cc}	–	4.75	5.00	5.25	volts
I_{cc}	5vdc	–	412	573	mA
V_{cc}	–	11.4	12.0	12.6	volts
I_{cc}	12vdc	–	76	100	mA
V_{cc}	–	-11.4	-12.0	-12.6	volts
I_{cc}	-12vdc	–	72	92	mA

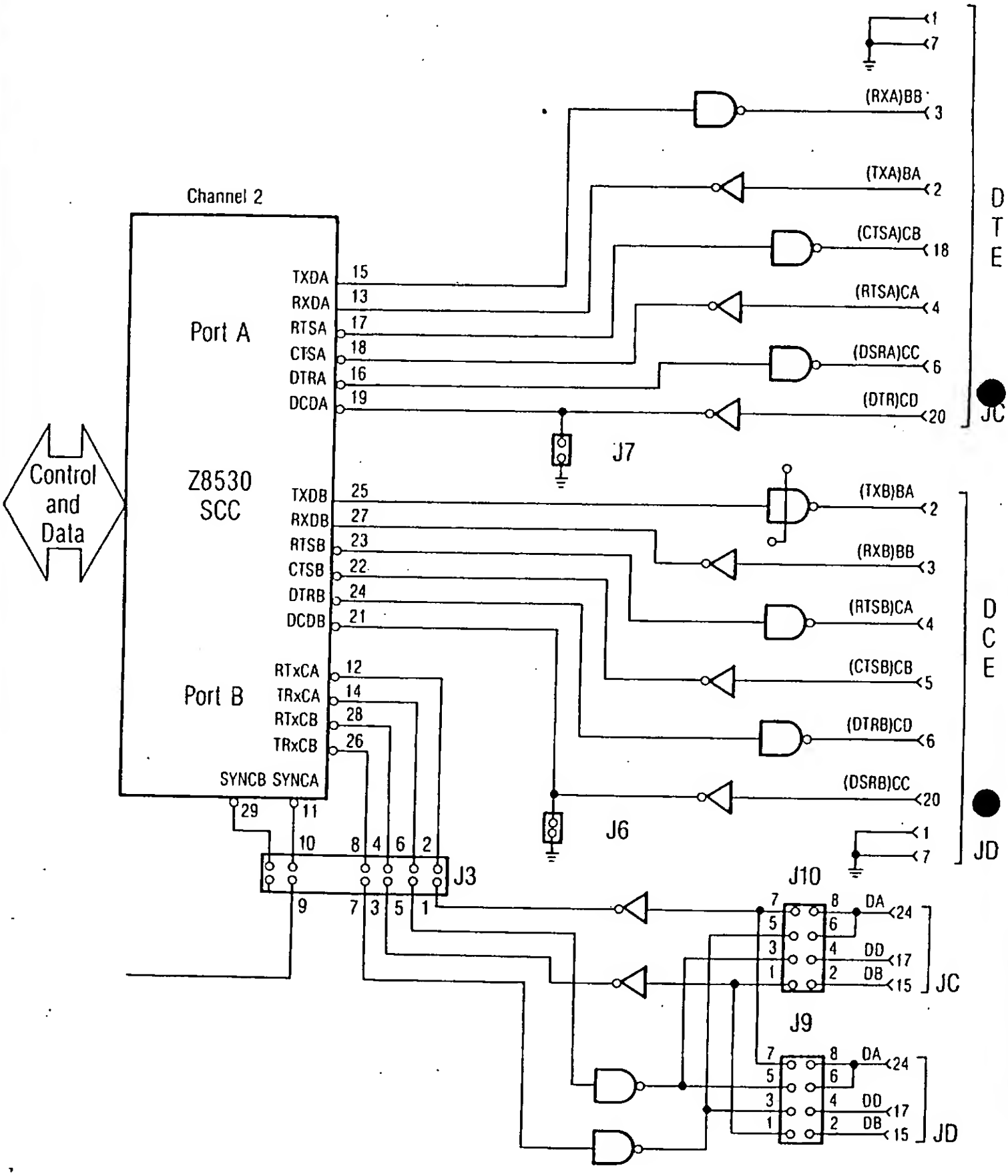
MECHANICAL

- ☐ Card Dimensions:

Form Factor	H	W	L	Units
STD-Bus	0.60	4.5	6.5	inches

- ☐ PC Board Thickness: 0.062 inches
- ☐ Connectors:
  STD-Z80 Bus: 56-pin, 0.125 inch centers
  Serial: 26-pin, dual row, 0.100 inch grid


Channel 1
Control and Data
Z8530 SCC
Port A
Port B
TXDA
RXDA
RTSA
CTSA
DTRA
DCDA
TXDB
RXDB
RTSB
CTSB
DTRB
DCDB
RTxCA
TRxCA
RTxCB
TRxCB
SYNCB SYNCA
15
13
17
18
16
19
25
27
23
22
24
21
12
14
28
26
29
11
J12
J11
J8
J5
J4
Y1
15PF
15PF
+5
8
Optional Oscillator
(RXA)BB
(TXA)BA
(CTSA)CB
(RTSA)CA
(DSRA)CC
(DTR)CD
(TXB)BA
(RXB)BB
(RTSB)CA
(CTSB)CB
(DTRB)CD
(DSRB)CC
DTE
JA
DCE
JB
DA
DD
DB
24
17
15


Channel 2
Control and Data
Z8530 SCC
Port A
Port B
TXDA
RXDA
RTSA
CTSA
DTRA
DCDA
TXDB
RXDB
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CTSB
DTRB
DCDB
RTxCA
TRxCA
RTxCB
TRxCB
SYNCB
SYNCA
(RXA)BB
(TXA)BA
(CTSA)CB
(RTSA)CA
(DSRA)CC
(DTR)CD
(TXB)BA
(RXB)BB
(RTSB)CA
(CTSB)CB
(DTRB)CD
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DTE
DCE
JC
JD
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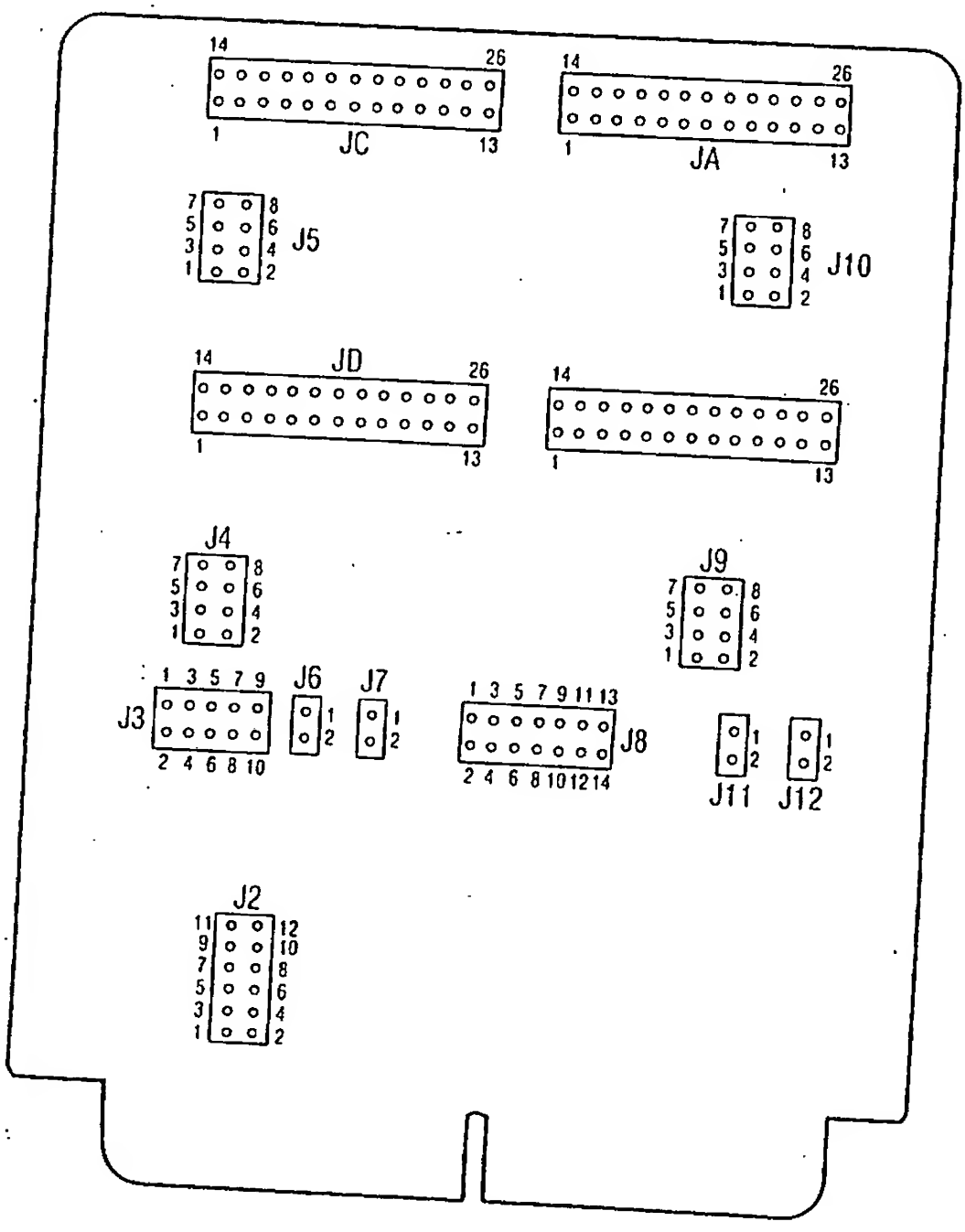
J6
J7
J9
J10
DA
DD
DB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1
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JC
JA
7
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8
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J5
J10
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J4
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1 3 5 7 9
2 4 6 8 10
J6
J7
1 3 5 7 9 11 13
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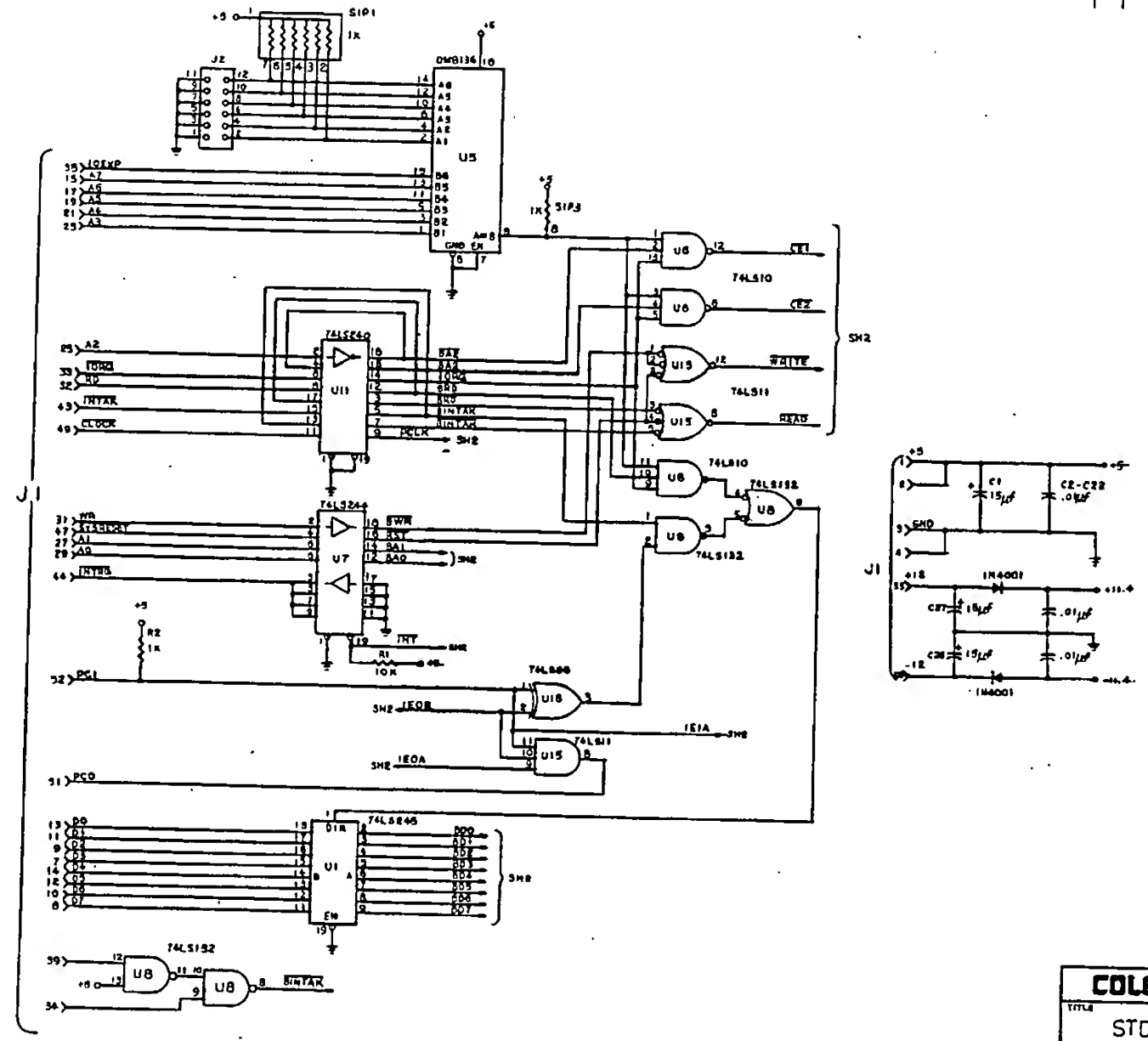
6
4
2

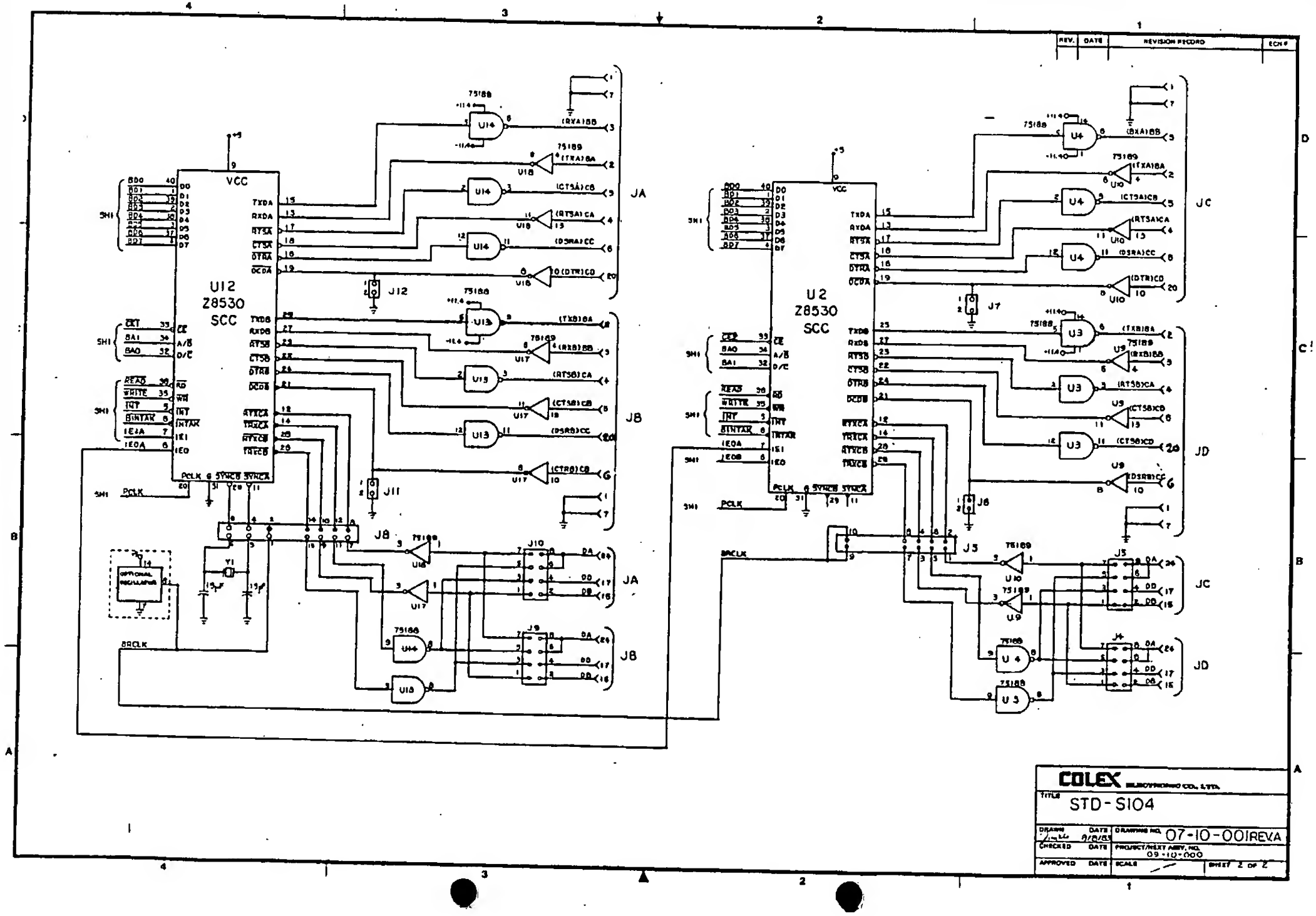


REV.	DATE	REVISION RECORD	ECN #

COLEX ELECTRONICS CO., LTD.

TITLE: STD-S104

DRAWN	DATE 10/8/82	DRAWING NO. 07-10-001REV.A
CHECKED	DATE	PROJECT/NEXT ASSY. NO. C9-10-000
APPROVED	DATE	SCALE — SHEET 1 OF 2


REV. | DATE | REVISION RECORD | ECN #
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SCC
U2
Z8530
SCC
VCC
PCLK & SYNCB SYNCA
BRCLK
OPTIONAL
J12
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J6
J5
J4
JA
JB
JC
JD
U14
U18
U13
U17
U4
U10
U3
U9
75188
75189
COLEX
TITLE
STD-SIO4
DRAWN
CHECKED
APPROVED
DATE
DRAWING NO. 07-10-001REVA
PROJECT/NEXT ASSY. NO.
09-10-000
SCALE
SHEET 2 OF 2